Remarks:

Reconsideration of the application is requested.

Claims 1-13 and 15-39 are now in the application. Claims 1, 15-27, 29, and 30 have been amended.

In item 3 on page 2 of the above-identified Office action, the Examiner noted the objection by the draftsperson. The objections have been noted and a better copy of the drawings will be provided upon receipt of a notice of allowance. This should be acceptable since no substantive changes are required.

In item 6A on page 3 of the Office action, claims 1, 7, 9-13, and 28 have been rejected as being anticipated by Bate (4,360,900) under 35 U.S.C. § 102.

The passage in column 5, lines 27 to 30 of Bate, which has been cited by the Examiner, does not refer to the memory layer structure. The titanium dioxide layer 25, 45 mentioned in line 16 is an intermediate layer between the aluminum layer 26 provided as the gate electrode and the memory layer structure used to store charge carriers and comprising an Si_3N_4 layer 23, 43 as a storage layer. This is clearly shown in Figures 4 and 8. The paragraph in column 5 following line 15 clearly describes that the purpose of this intermediate layer and of

the chosen materials is to shift the main voltage drop into the storage layers. The storage layers comprise standard sequences of silicon oxide and silicon nitride. The claimed special embodiments comprise storage layers and boundary layers, instead, which are formed of the special materials listed in the description and also given by Bate.

Claim 1 and 27, however, have been amended to better define the invention. Support for the changes can be found by referring to claim 14, to the figures, and the specification on page 10, lines 22 to 24. Notably, the channel length can only be optimized by means of the depths of the trenches, if there is no source or drain region arranged at the bottom.

Claim 1 now specifies a memory cell comprising:

a semiconductor component having semiconductor material and a top side, said semiconductor component selected from the group consisting of a semiconductor body and a semiconductor layer, said semiconductor material having a surface;

a memory transistor including a source region and a drain region that are formed at said surface of said semiconductor material, said memory transistor including a gate electrode located on said top side and located between said source region and said drain region;

a dielectric material separating said gate electrode from said semiconductor material; and

a layer sequence including boundary layers and a memory layer located between said boundary layers, said layer sequence located at least between said source region and said gate electrode and at least between said drain region and said gate electrode;

said semiconductor material having a trench formed therein and said gate electrode located in said trench.

Claim 27 defines a memory cell configuration, comprising:

a semiconductor component having semiconductor material and a top side, said semiconductor component selected from the group consisting of a semiconductor body and a semiconductor layer, said semiconductor material having a surface;

a plurality of memory cells that each include:

a memory transistor including a source region and a drain region that are formed at said surface of said semiconductor material, said memory transistor including

a gate electrode located on said top side and located between said source region and said drain region;

a dielectric material separating said gate electrode from said semiconductor material; and

a layer sequence including boundary layers and a memory layer located between said boundary layers, said layer sequence located at least between said source region and said gate electrode and at least between said drain region and said gate electrode; and

a plurality of conductor tracks defining word lines, said gate electrode of each one of said plurality of said memory cells electrically conductively connected to one of said plurality of said conductor tracks;

said source region of one of said plurality of said memory cells defining said drain region of an adjacent one of said plurality of said memory cells and said drain region of said one of said plurality of said memory cells defining said source region of another adjacent one of said plurality of said memory cells;

said semiconductor material has a plurality of trenches formed therein;

said gate electrode of each one of said plurality of said memory cells is located in a respective one of said plurality of said trenches.

Bate does not teach a structure having a gate electrode configured between source and drain regions. Bate teaches planar devices as can be seen in figs. 3a and 7a thereof. The source and drain regions are formed in the substrate, whereas the gate electrode is formed by a layer located above the source and drain regions.

In item 6B on page 5 of the Office action, claims 1-6, 8-10, 12-19, 21, 23-25, and 26 have been rejected as being anticipated by Hofmann et al. (6,191,459) under 35 U.S.C. § 102.

Claim 1 includes a memory transistor including a source region and a drain region that are formed at the surface of the semiconductor material. The semiconductor material has a trench formed therein and the gate electrode is located in the trench.

Hofmann et al. do not teach a structure having a gate electrode configured between source and drain regions that are formed at the same surface. Hofmann et al. disclose a memory

cell array comprising source and drain regions that are alternatively situated at the upper surface of the semiconductor body and at the bottom of trenches formed therein. The inventive structure uses the trench bottoms as channel regions.

In item 7A on page 7 of the Office action, claim 29 has been rejected as being obvious over Bate (4,360,900) in view of Hofmann et al. (6,191,459) under 35 U.S.C. § 103.

Claim 29 is patentable for the reasons discussed above with regard to the anticipation rejection of claim 27 in light of Bate (4,360,900).

In item 7B on page 8 of the Office action, claims 20 and 24 been rejected as being obvious over Hofmann et al. (6,191,459) in view of Bate (4,360,900) under 35 U.S.C. § 103.

Claims 20 and 24 are patentable for the reasons discussed above with regard to the anticipation rejection of claim 1 in light of Hofmann et al. (6,191,459).

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 or 27. Claims 1 and 27, therefore, believed to be patentable over the art and

since all of the dependent claims are ultimately dependent on claim 1 or 27, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-13 and 15-32 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, he is respectfully requested to telephone counsel so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any other fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicants

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